

Cree *Z-REC™* 1700V Schottky Diode Chips CPW3-1700-S010B and CPW3-1700-S025B

Qualification Report

Summary

This report documents the qualification and reliability test results for the 1700 V breakdown rated SiC Schottky diode chip products CPW3-1700-S010B (10 Amp) and CPW3-1700-S025B (25 Amp), fabricated on SiC substrates (nominally 100 mm or smaller) at Cree, Inc., Durham, North Carolina, USA. Zero device failures were observed out of 1004 total devices evaluated in a variety of qualification and reliability stress tests. The results qualify the products for volume manufacturing.



Qualification Plan

Test Descriptions

Parametric Verification (PV)

Parametric Verification (PV) is used to evaluate whether the devices tested meet performance specifications as listed on the product data sheet. The process capability index (Cpu for unilateral upper specification limits and Cpl for lower specification limits) is a statistical measure of the capability of the process to produce devices within the specification limits.

External Visual (EV)

EV will utilize an automated, high-power visual inspection tool to identify external defects associated with the chip.

Unbiased Autoclave (AC)

AC testing is used to evaluate resistance to Galvanic and direct corrosion in a high moisture environment.

High Humidity, High Temperature Reverse Bias (H3TRB)

H3TRB testing is used to evaluate resistance to Galvanic, electrochemical and direct corrosion, as well as ionic migration, in a high moisture and temperature environment as well as high electric field.

High Temperature Reverse Bias (HTRB)

HTRB testing is used to evaluate reliability under high electric field and temperature.

Temperature Cycle (TC)

TC will accelerate damage caused by thermal-mechanical stress as a result of thermal mismatch and dimensional differences.

Intermittent Operating Life (IOL)

IOL testing is designed to evaluate resistance to damage caused by thermal-mechanical stress as a result of thermal mismatch associated with local thermal gradients within the chip caused by internal power dissipation.

Electrostatic Discharge (ESD)

ESD ratings are established for human body model (HBM) and charged device model (CDM).



Test Plan

The product qualification test plan outlined Table 1 is based on the guidelines of AEC-Q101, Stress Test Qualification for Automotive Grade Semiconductors, and references therein. The devices are to be randomly sampled from three wafer lots. For testing purposes, the chips were assembled in gold-plated TO-247 packages. However, only the chip product is being qualified. The packaging solution is not being qualified.

Table 1: Qualification Test Plan

Test	Sample Size per Lot	# of Lots	Test Vehicle	Stress Conditions	Acceptance Criterion
PV	17	3	10 A (25 DUTs) and 25 A (25 DUTs)	n/a	Cpu \geq 1.33 (4 σ)
EV	All chips used for qualification	All chips used for qualification	10A and 25A	n/a	Pass inspection criteria
AC	25	3	25 A (75 DUTs)	96 hours, 121 °C, 100% RH, 205 kPa	0 fail
H3TRB	77	3	10 A (78 DUTs) and 25 A (154 DUTs)	1000 hours at 85 °C, 85% RH with device reverse biased at 100 V	0 fail
HTRB	77	3	10 A (77 DUTs) and 25 A (154 DUTs)	1000 hours at 150 °C with device reverse biased to 1360 V (80% of max)	0 fail
TC	77	3	Two 25 A die per package with silicone potting	1000 cycles, -55 °C to 150 °C, JEDEC A104 condition H, soak mode 1	0 fail
IOL	77	3	10 A (78 DUTs) and 25 A (156 DUTs)	6000 cycles, 3.5 minutes on / 3.5 minutes off*, $\Delta T_j \geq 100$ °C	0 fail
ESD-HBM	30	1	10 A	Ramp per AEC-Q101	Characterization
ESD-CDM	30	1	10 A	Ramp per AEC-Q101	Characterization

*The on and off times were reduced compared to the AEC recommended guideline of 5 minutes on / 5 minutes off because the thermal response times of the chip and package are significantly faster than those dwell times.



Device Failure Criteria

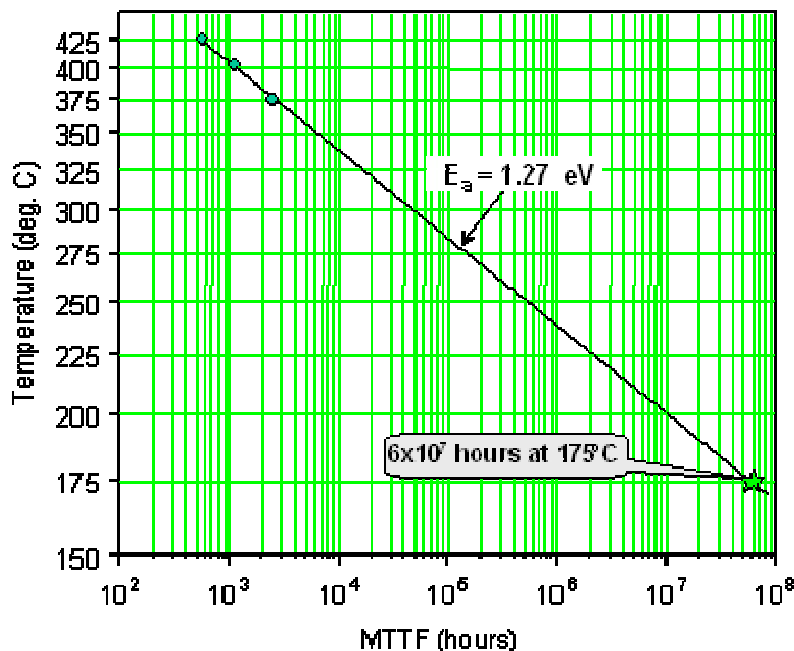
A device failure is defined as a condition in which a stressed device can no longer meet its data sheet specifications, or has consequential external physical damage attributable to an environmental test.

A determination of root cause will be made immediately for any failure found. If the root cause of failure is mishandling, test equipment failure, or a data acquisition failure, the failing devices will be removed from the test, and not counted as a qualification failure. If time constraints regarding test suspension are not violated, the qualification test will resume with the remaining devices so long as the total number of remaining devices is at least 90% of the starting sample size (per lot).

A single failure that cannot be identified within the time constraint for a suspended test, or is identified as an inherent device failure, will constitute a qualification failure for the test at hand and noted in the final qualification report. Other qualification tests may proceed so long as their results are not likely to be significantly impacted by the corrective action required by the identified failure mode. This determination will be made by the reliability manager responsible for the product qualification.

Intrinsic Reliability

The intrinsic reliability performance is qualified by similarity to previously qualified SiC MESFETs. Previous studies on the SiC MESFETs have shown that the wear-out intrinsic reliability failure mechanism is Ohmic contact degradation under high current and temperature conditions. The Cree SiC Schottky diodes all utilize the same Ohmic contact structures as the SiC MESFETs. Accelerated life testing of Ohmic test structures resulted in an activation energy of 1.3 eV and intrinsic lifetime projection of 6×10^7 hours (60% lower confidence limit = 4.3×10^7 hours) for continuous operation under forward bias at the maximum junction temperature of 175°C , as shown in the figure below.





Qualification Test Descriptions and Results

Parametric Verification

The tables below show the results of parametric verification testing. The resulting Cpu/Cpl values all meet or exceed the target value of 1.33.

Table 2: Parametric Verification Results CPW3-1700-S010B at 25°C
*Could not be quantified due to test equipment limitations.

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPU/CPL
VF (Rated Current)	V		2.0	1.61	1.68	1.65	0.02	6.5
IR at 1700 V	μA		50	0.2	7.0	2.0	2.0	8.74
VBR at 10 μA	V	1700		n/a*	>2000	>2000	n/a	n/a

Table 3: Parametric Verification Results CPW3-1700-S010B at 175°C
*Could not be quantified due to test equipment limitations.

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPU/CPL
VF (Rated Current)	V		3.5	2.77	3.14	3.0	0.1	1.69
IR at 1700 V	μA		200	8	54	14	10	6.39
VBR at 10 μA	V			n/a*	>2000	>2000	n/a	n/a

Table 4: Parametric Verification Results CPW3-1700-S025B at 25°C
*Could not be quantified due to test equipment limitations.

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPU/CPL
VF (Rated Current)	V		2.0	1.69	1.87	1.79	0.05	1.41
IR at 1700 V	μA		100	0.2	7	2.0	1.9	17.18
VBR at 10 μA	V	1700		n/a*	>2000	>2000	n/a	n/a

Table 5: Parametric Verification Results CPW3-1700-S025B at 175°C
*Could not be quantified due to test equipment limitations.

TEST NAME	UNIT	SPEC LSL	SPEC USL	MIN	MAX	MEAN	STD.DEV.	CPU/CPL
VF (Rated Current)	V		4.0	2.93	3.52	3.2	0.2	1.36
IR at 600 V	μA		400	11	76	32	15	7.9
VBR at 10 μA	V	1700		n/a*	>2000	>2000	n/a	n/a

External Visual

No visual anomalies were observed during External Visual inspection on any of the die used for qualification.



Reliability

Table 6 shows the results of the reliability testing. Zero chip failures were observed for all electrical and environmental stress tests conducted. Zero chip failures were observed up to the maximum recommended levels for ESD-HBM and ESD-CDM, which results in the highest ESD rating classification for both test methodologies.

Table 6: Reliability Qualification Results Summary

Stress	Failures	Result
AC	0/75	Pass
H3TRB	0/231	Pass
HTRB	0/231	Pass
TC	0/231	Pass
IOL	0/231	Pass
ESD-HBM	All devices passed 8000V	Class H3B (>8000V)
ESD-CDM	All devices passed 1000V	Class C5 (>1000V)

Conclusion

The 1700 V breakdown rated SiC Schottky diode chip products CPW3-1700-S010B (10 Amp) and CPW3-1700-S025B (25 Amp) are qualified for volume manufacturing, as a result of parametric verification, external visual inspection, and zero failures out of the qualification plan for electrical and environmental reliability and ESD stress.