

# Comprehensive First-Pass Design Methodology for High Efficiency Mode Power Amplifier

■ David Yu-Ting Wu and Slim Boumaiza

The wireless technology evolution has consistently focused on increasing data rate and user mobility while keeping overall cost at bay. The quest for higher data rates has led to increased spectral utilization in new standards with unfortunate tradeoffs such as rapidly varying signals and high peak-to-average power ratio. To preserve linearity, existing RF PAs are operated with reduced input drive, where the PAE decreases significantly. The low PAE causes emerging handsets to exhibit shorter battery life and base stations to possess higher carbon footprints along with major cooling requirements. As such, research on increasing peak efficiency of RF PAs using novel classes of operation such as Class F, Class E, and Class D [1] coupled with efficiency enhancement techniques at reduced input drive (e.g., the Doherty PA [2]) has attracted considerable attention.

Despite their advantages and successful implementations in the literature, high-efficiency PAs have yet to see large-scale adoption, in part due to their strong nonlinearity. Fortunately, research on digital predistortion and advanced transmitters utilizing nonlinear PAs, such as envelope tracking and polar transmitters, have begun to mitigate these concerns.

Perhaps the most significant barrier to large-scale adoption not often addressed is the lack of first-pass design methodology. Despite well-established theory, practical PA implementations are often empirical in nature, where experience and extensive post-production tuning is used to achieve the desired amplifier characteristics. While such

an approach combined with thorough theoretical understanding is useful in illustrating RF device potentials, it becomes less relevant in pushing for large-scale adoption, since mass production depends on first-pass design without costly post-production tuning.

In this paper, such a first-pass design methodology is presented, taking advantage of the arrival of highly accurate large signal device models. Using the method described, an inverse Class F PA with minimum tuning is realized, measuring 71% PAE at 3.27 GHz at the 2009 IMS Student Design Competition.

## Theory of Operation and Design Specifications

The theory behind high-efficiency modes such as Class F and Class E is described well in previous literature [3]–[4]. The key to high-efficiency operation lies in engineering the output waveform such that the instantaneous voltage and current exhibit minimum overlap, since any overlap leads to power dissipation in the transistor and reduces the dc-to-RF conversion efficiency.

**Research on digital predistortion and advanced transmitters utilizing nonlinear PAs have begun to mitigate the concerns about nonlinearity.**

Figure 1 illustrates a set of nonoverlapping voltage and current waveforms, representing the ideal inverse Class F output. Fourier analysis reveals that the square wave and half-sine wave consist of odd and even harmonics, respectively, thus highlighting the importance of harmonic content in realizing nonoverlapping waveforms. It turns out the often undesirable nonlinear characteristic of the transistor can be cleverly exploited to supply the harmonics required. Engineering the level of nonlinearity generated by the transistor

is achieved through proper selection of bias point and input drive level. The use of open or short impedance terminations at the harmonic frequencies then act to filter the respective waveforms to contain only odd or even Fourier terms, thus achieving the nonoverlapping square and half-sine waves.

High-efficiency PA design is therefore about synthesizing a matching network having impedances that can leverage the inherent transistor nonlinearity to obtain nonoverlapping waveforms at the transistor intrinsic drain.

For the competition, the maximum input drive was 25 dBm, thus a device with sufficient nonlinearity at this input level was selected. The Cree CGH40010 GaN transistor met this requirement along with excellent gain and matching characteristics at the design frequency of 3.3 GHz. The transistor was biased at  $V_{ds} = 28$  V and  $I_{ds} = 200$  mA in deep Class AB.

## Determining Matching Network Impedances

Practical implementation of high-efficiency PAs face some complications not usually considered in theory. Figure 2

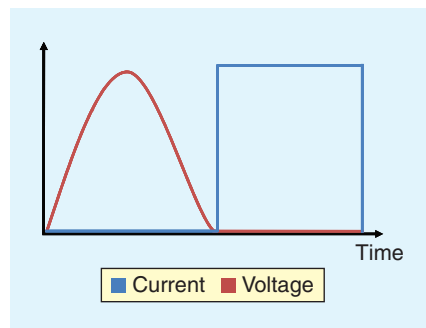


Figure 1. Ideal inverse Class F voltage and current waveforms.

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depicts a simplified transistor equivalent circuit with device parasitic and packaging. As shown, the transistor intrinsic drain, where the nonoverlapping waveform should be realized, is physically inaccessible due to the output parasitic and device packaging. Instead, the matching network is connected at the package reference plane where there exists a frequency-dependent phase shift from the intrinsic drain.

Thus, the set of impedances at the package reference plane resulting in non-overlapping waveforms at the intrinsic drain needs to be determined, a difficult analytical task without exact knowledge of the package and parasitic.

In light of this difficulty, a technique known as load pull is used, where impedances on the input and output of the packaged transistor are varied until high efficiency is achieved. Figure 3 contains the optimal input and output impedances found by load and source pull up to the third harmonic using the Cree large-signal model.

In order to determine the class of operation, the output waveforms at the package reference plane are de-embedded first with the device package supplied by Cree. Next, the device parasitic in Figure 2 is determined from analysis of the transistor under zero bias condition (i.e.,  $V_{ds} = 0$ ), also known as the cold field-effect transistor (FET) technique [5]. Upon de-embedding the output parasitic, the waveforms at the intrinsic drain are extracted. Figure 4 illustrates the de-embedded waveforms with square current and half-sine voltage waveforms, indicating inverse Class F operation.

### PAE Sensitivity Analysis

Upon determining the optimal impedances, microstrip matching networks are designed to present these impedances to the transistor. However, the realized matching network impedances are always subject to errors due to manufacturing tolerance, variation in substrate dielectric, imperfect soldering, and other factors unaccounted for in simulation. It is therefore prudent to conduct a PAE sensitivity analysis as a function of input and output impedances to determine the impact

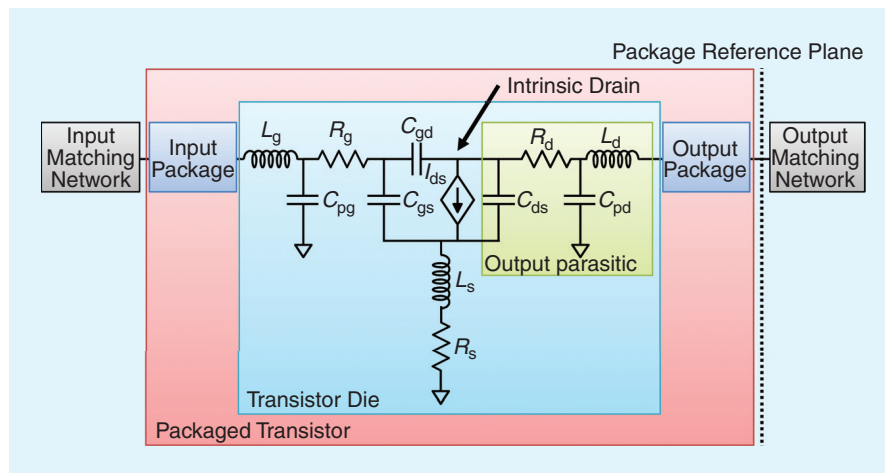


Figure 2. Transistor equivalent circuit showing parasitics and device packaging.

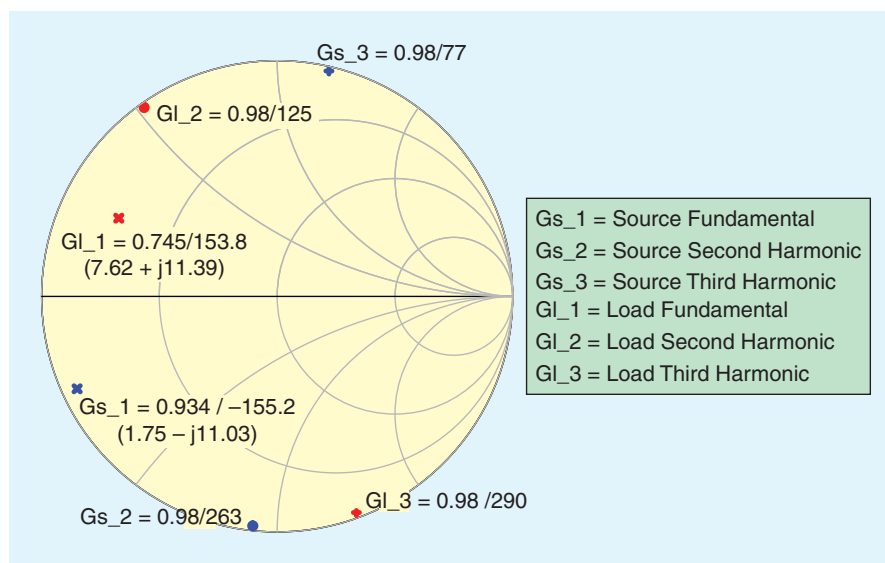


Figure 3. Optimal impedances yielding maximum power added efficiency determined by load pull and source pull.

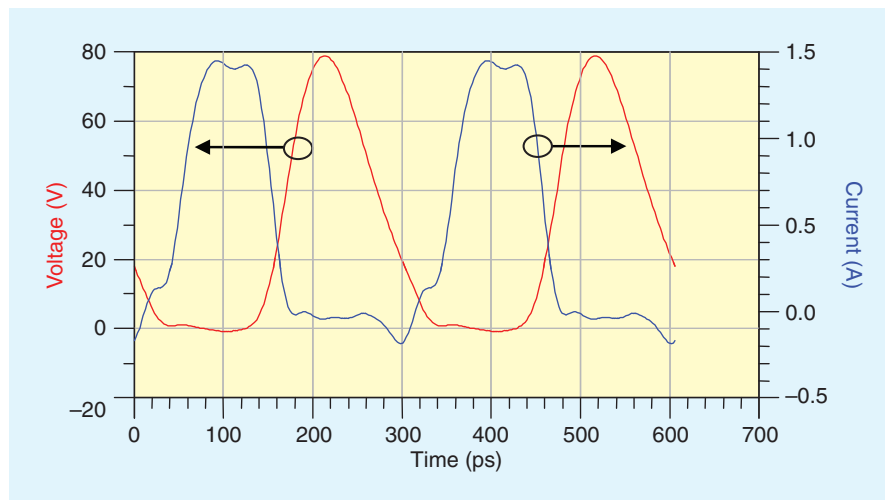
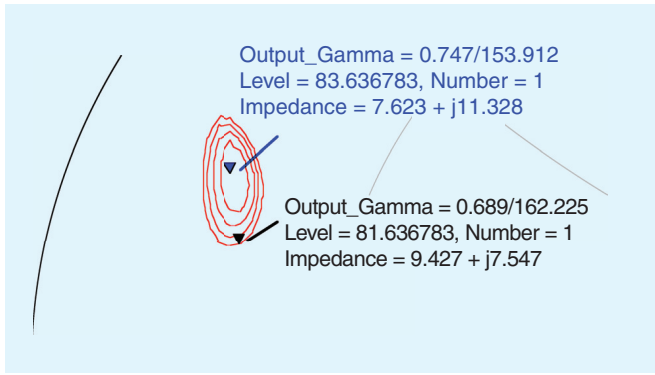
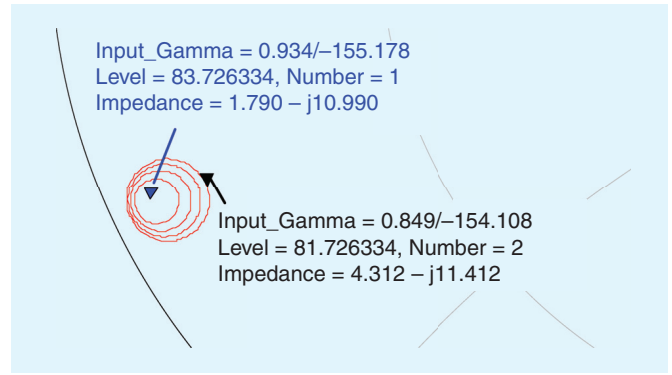


Figure 4. De-embedded waveforms indicating inverse Class F operation.



**Figure 5.** Output impedance power added efficiency contours indicating a large region of impedance tolerance.



**Figure 6.** Input impedance power added efficiency contours revealing the trade-off between higher input impedance and efficiency.

on efficiency due to errors in matching network impedance realization. Such analysis can also determine whether PAE is a function of input harmonic terminations, since traditionally only output harmonic terminations are considered in both theory and practice.

In Figures 5 and 6, output and input fundamental impedances [expressed with reflection coefficient  $\Gamma = (Z - Z_o) / (Z + Z_o)$ ], where  $Z_o$  is the characteristic impedance are varied on the Smith chart to generate PAE con-

tours in steps of 0.5%, with the largest contour 2% below maximum.

On the output fundamental, a large high-efficiency region with ample amplitude and phase tolerance for  $\Gamma$  is observed. Given this, matching network synthesis using an accurate electromagnetic simulator will ensure that the realized impedance will be in this region even with the aforementioned uncertainties.

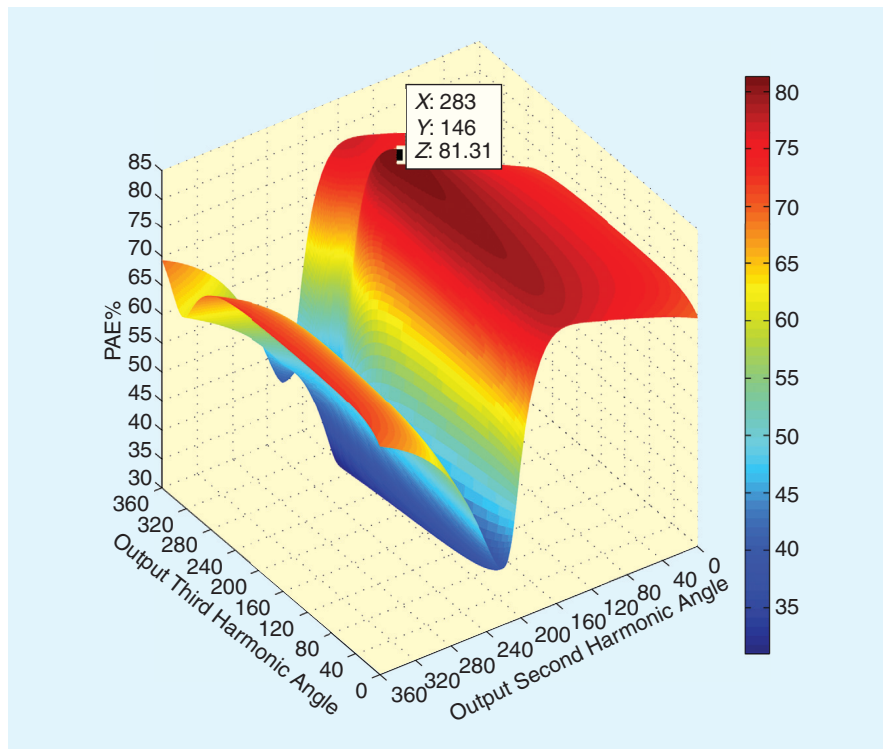
On the input fundamental, an impedance of approximately  $1.8 \Omega$  was required. Matching such a low imped-

ance to  $50 \Omega$  is difficult and usually results in designs with high sensitivity to manufacturing tolerance and large insertion loss. Therefore, a design tradeoff was made, where the input impedance was increased slightly (from blue to black marker in Figure 6) to reduce both matching network insertion loss and sensitivity to manufacturing tolerance. The load pull process was repeated to yield a new set of optimal impedances incorporating this tradeoff.

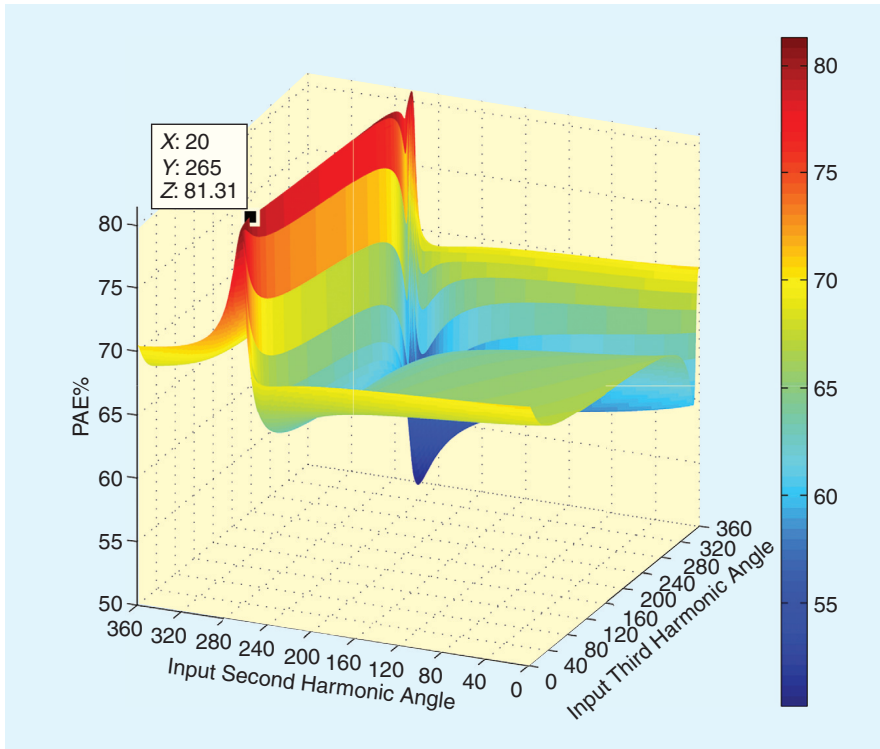
Figures 7 and 8 illustrate in three dimension (3-D) the effects on PAE when the phase of the second and third harmonic reflection coefficients  $\Gamma_h$ , were swept at the edge of the Smith chart (i.e.  $|\Gamma_h| = 0.98$ ). The sweeps were accomplished in simulation using programmable load generator with fundamental impedance fixed at the optimal value.

As with the output fundamental, the output harmonics show a large region of impedance tolerance indicated by the red plateau. However, the input harmonics show a very surprising result, with PAE being extremely sensitive to the input second harmonic termination. Figure 9, an extraction of Figure 8 at the optimal third harmonic termination, indicates that a reflection coefficient phase range of only four degrees yields PAE above 80%. The decrease in PAE is rapid and asymmetric about the optimal point, with most regions exhibiting PAE below 70%.

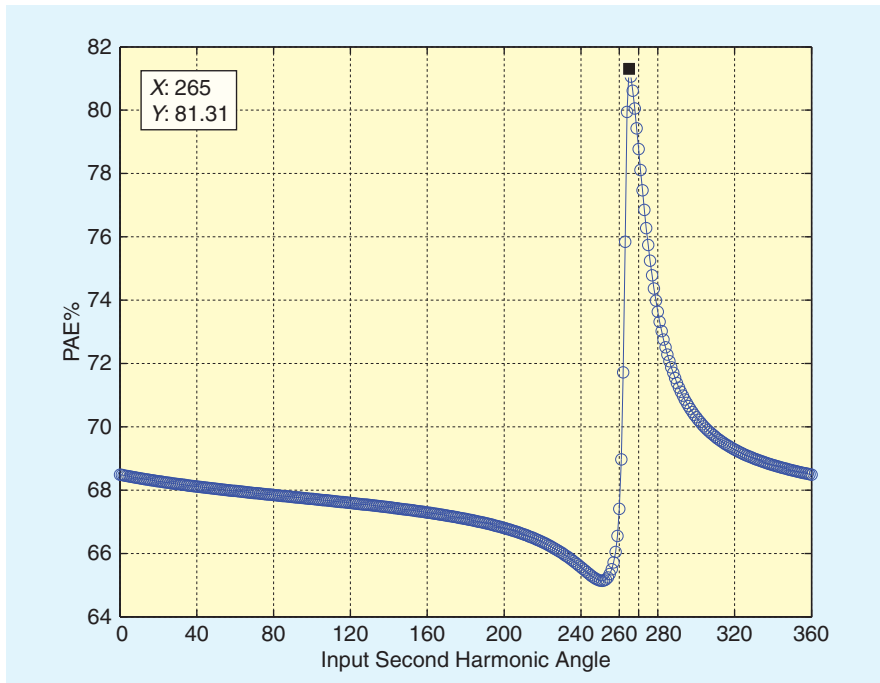
The cause of extreme sensitivity due to the input second harmonic termination is not well understood



**Figure 7.** Power added efficiency sensitivity analysis as a function of the output second and third harmonic reflection coefficient phase angle.



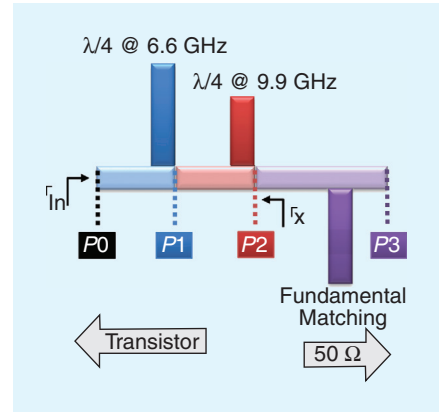
**Figure 8.** Power added efficiency sensitivity analysis as a function of the input second and third harmonic reflection coefficient phase angle.



**Figure 9.** Power added efficiency versus the input second harmonic angle extracted at the optimal third harmonic angle.

and requires further investigation. The phenomenon was verified in real devices using multiharmonic load pull, thus it is not a modeling error. The sensitivity to the input second harmonic

termination left little design tolerance and posed a significant challenge since poor soldering alone can shift the second harmonic reflection coefficient phase at 6.6 GHz by  $10^\circ$ . Therefore,



**Figure 10.** Diagram illustrating the matching network design process.

presenting the exact harmonic termination phase to the transistor will be very difficult.

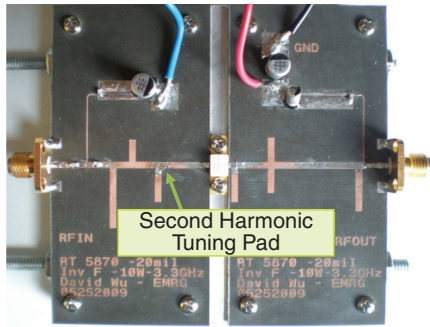
Finally, the effect on PAE due to reduction in the magnitude of the harmonic reflection coefficient  $|\Gamma_h|$  was investigated, while  $\Gamma_h$  phase was kept at the optimal value. Table 1 indicates that PAE is adversely affected by decreasing the second harmonic magnitude, but not by the third harmonic. The lack of third harmonic impact generally observed can be attributed to the device capacitance which, at 9.9 GHz, is essentially a short. Therefore, external harmonic control yields very little effect.

### Matching Network Design

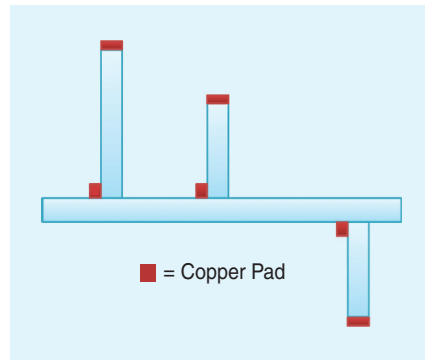
The objective in matching network design is the accurate synthesis of required impedances with the lowest insertion loss possible. Insertion loss, especially on the output, decreases the PAE drastically and is minimized by choosing a low-loss substrate and appropriate matching network topology. As illustrated in Figure 10, the fundamental matching is implemented with single or double stub matching while harmonic terminations are realized using quarter-wave open-circuit stubs. It can be shown that the harmonic stub closest to the transistor will have the highest  $|\Gamma_h|$ . Therefore, in order to achieve the highest PAE in accordance with Table 1, the matching network terminates the second harmonic before the third harmonic. At each T-junction, the quarter-wave harmonic open-stub

**TABLE 1. Power added efficiency sensitivity analysis as a function of magnitude of harmonic termination.**

$ \Gamma_h $	Source_2f0	Source_3f0	Load_2f0	Load_3f0
0.98	81.42%	81.42%	81.42%	81.42%
0.95	79.56%	81.42%	80.77%	81.30%
0.92	77.89%	81.42%	80.11%	81.19%
0.89	76.60%	81.41%	79.46%	81.08%



**Figure 11.** Photograph of the fabricated power amplifier showing the input and output matching networks.

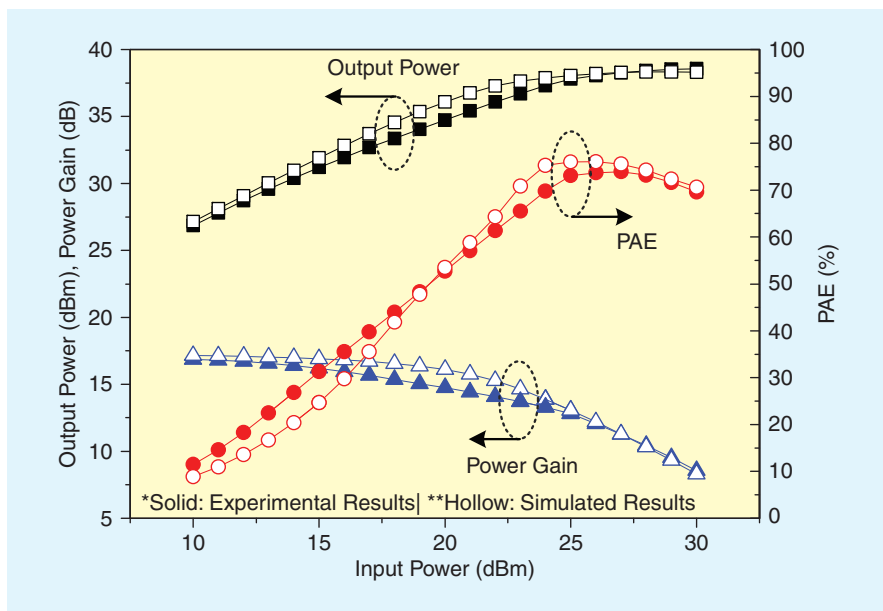


**Figure 12.** Copper tuning pads placed in the simulations.

transforms to a short in parallel with the rest of the circuit, thus, isolation is created between each harmonic termination and the circuitry to follow. This allows for a straightforward, three-step design process that can utilize an electromagnetic simulator directly.

The design procedure is illustrated in Figure 10 with the transistor and 50  $\Omega$

termination connected at port P0 and P3, respectively. The second-harmonic termination is synthesized by placing 50  $\Omega$  terminations at port P0 and P1. Then, starting from the short circuit on the Smith chart, the light blue transmission line is increased until reaching the optimal second harmonic phase.  $S_{21}$  between P0 and P1 should be



**Figure 13.** Power amplifier measurement and simulation results showing power added efficiency, output power, and gain as function of the input power.

at least  $-30$  dB to ensure isolation from subsequent circuitry. The process is repeated for the third harmonic using the light red transmission line with reference port at P0 and P2. Finally, the conjugate of the required fundamental impedance is placed at P0 and  $\Gamma_x$ , the impedance matching requirement at the fundamental given the presence of the harmonic control circuitry, is determined. The purple fundamental matching network is then designed to match  $\Gamma_x$  to 50  $\Omega$ , completing the matching network synthesis.  $\Gamma_{inv}$ , the impedance seen by the transistor, now presents the required impedance at the fundamental and harmonics. To reduce insertion loss, open stubs approaching  $\lambda/4$  (at the fundamental frequency) are avoided in accordance with previous literature [6]. Figure 11 shows the fabricated PA with the input and output matching network designed using the synthesis technique described above.

### Advanced Tuning Technique

The initial performance of the fabricated PA was lower than expected. However, insight from the sensitivity analysis indicated that the input second harmonic termination was likely the culprit. To determine how to tune the matching network from simulation, copper pads, shown in Figure 12, were placed one at a time, and electromagnetic simulation revealed their effect on the fundamental and harmonic impedances.

The copper pad marked with an X was found to reduce the second harmonic reflection coefficient phase without affecting fundamental or third harmonic. Upon tuning the fabricated PA in this fashion, the optimal input second harmonic termination phase was obtained and maximum PAE was achieved. This tuning is reflected in Figure 11 and was the sole adjustment made to the fabricated matching networks.

### Simulation Versus Measurement Results

Simulations were conducted using the large-signal transistor model provided by Cree along with the designed input and output matching network in Agilent Advance Design System. The

## Timeline for the Competition

To prepare for the competition, initial work began in March 2009, three months before the competition, when the design frequency and transistor device were selected. For the next month or so, the authors calibrated a multi-harmonic load pull setup which confirmed the accuracy of the large-signal model in predicting the transistor performance. Thus, a decision was made to use the device model as the gold standard in designing the power amplifier. Design using the model enabled more analysis and design insight and proved to be a viable approach. The first design iteration showed good performance, but with the input third harmonic terminated before the second harmonic, this design had a lower PAE. On the second iteration, the winning entry was developed.

proprietary Cree model is based on a 13-element metal semiconductor FET (MESFET) model developed in [7]. Figure 13 shows the output power, PAE, and power gain as functions of input power. The measurements follow closely with simulation predictions, validating the accuracy of the transistor model. The peak PAE reduction from 81% to 74% was due to an output insertion loss of roughly 0.25 dB, reflected in both simulation and measurement. The final PA operating frequency was shifted slightly from 3.3 GHz to 3.27 GHz.

## Conclusion

In this paper, a first-pass methodology for designing a high-efficiency PA was presented. The techniques discussed, such

as PAE sensitivity analysis, matching network synthesis, and advanced tuning methods, were used to design the winning PA entry at the 2009 IMS Student Design Competition. The knowledge that PAE is extremely sensitive to the input second harmonic termination allowed for informed post-production tuning. The measurement results match the simulation closely, validating the model accuracy. Future work will include investigation of the input harmonic termination on PA efficiency and methods for achieving broader bandwidth in a high-efficiency PA.

## Acknowledgments

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and large-signal model and Agilent Technologies for donating the ADS design software. The authors would also like to thank Dr. Jangheon Kim for insights and discussions, as well as MTT-5 for hosting the Student Design Competition.

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## Overview of the LNA Student Competition

### ■ Roger Kaul

Five teams of students participated in the student competition for a LNA design at IMS 2009. The challenge was to design, construct and demonstrate the lowest noise figure amplifier at 2.45 GHz with at least 15 dB of gain operating in a 50- $\Omega$  system at room temperature.

Two tests of each amplifier were performed to ensure that no measure-

ment error occurred. One of the concerns of the judges was that two or more amplifiers would have noise figures that were statistically equal. If that case arose, the winner would be determined by selecting the amplifier with the lowest power consumption. Fortunately, this situation did not occur.

The judges were members of the four technical committees that sponsored the LNA competition and an application engineer from Rohde & Schwarz (R&S) who assisted with operating the equipment used to measure

the LNAs. Several test runs were made at the R&S facility in Columbia, Maryland, to ensure that the testing would go smoothly and be accurate. In addition, Noisecom provided a specially designed excess noise source calibrated for this frequency and suitable for low-noise figure measurements.

The four sponsoring technical committees were the Microwave and Millimeter-Wave Integrated Circuits (MTT-6), Microwave Low-Noise Techniques (MTT-14), Microwave Systems (MTT-16), and Wireless Communications (MTT-20).

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Roger Kaul is past chair of MTT-16.

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