Linearity Improvement in RF Power Amplifier System using Integrated Auxiliary Envelope Tracking System

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***Abstract* — A new technique called Auxiliary Envelope Tracking (AET) is proposed, which demonstrates substantial improvement in linearity of RF power amplifiers. A small amplitude envelope-tracking voltage is superimposed on the fixed DC bias of a specially designed 25W GaN HEMT Class AB RF power amplifier (RFPA). A large improvement in third-order intermodulation (IM3) distortion has been observed while maintaining low fifth-order intermodulation (IM5). The overall drain efficiency of the RFPA is also observed to improve, even when the power consumption of the envelope tracking generator is included. The AET concept uses a simple and easily integrated system that consists of an RFPA, a diplexer and an envelope amplifier.**

***Index Terms* — Linearization techniques, Power amplifiers, Intermodulation, Gallium nitride (GaN).**

I. Introduction

Advance digital communications systems place increasing demands on RFPA efficiency and linearity. There are a number of linearization techniques that have been extensively researched and well documented in the literature [1]-[3] namely, feed-forward, feedback and pre-distortion. All of these techniques however add significant complexity and cost to the system design.

Here, we propose a new linearization technique that we call Auxiliary Envelope Tracking (AET), which can be applied to any RFPA. The name of this technique is derived from the regular Envelope Tracking (ET) system that is a well-known efficiency enhancement technique for power amplifiers. However, here, the emphasis of the AET system is on linearity improvement. The basic operation has some similarities to regular ET. In AET, the RF input signal is split into RF and envelope paths. The RF signal on the envelope path is detected and amplified by a low frequency envelope amplifier before this signal is injected into the drain port of the RF PA via a diplexer. In this AET, the combined injected amplified envelope signal and dc component is called AET signal. In regular ET, the envelope tracking drain bias signal will improve the efficiency, but only if the tracking voltage generator is itself highly efficient (>80%). In the AET system however, the combination of the tracking drain bias signal with the characteristic of the GaN HEMT device gives a major improvement in the linearity of the power amplifier. This AET system also has the potential to present a simple and low cost solution to linear-efficient RFPA design. The additional circuitry involves a simple diplexer and a low cost envelope amplifier. In our ongoing work, we believe AET can be used not only for linearity improvement but also for significant efficiency enhancement.

II. Characteristic of GaN HEMT Device and Linearity Analysis

The concept of using AET to improve linearity was motivated by observing the gain characteristic of a Gallium nitride (GaN) high electron mobility transistor (HEMT) power device. A 25W GaN HEMT Class AB power amplifier was designed and the performance of this amplifier was measured. The gain of the amplifier was observed to change in an approximately linear fashion with the drain supply voltage on a decibel scale as shown in Fig. 1. This positive slope of gain is the basic property that is used here to improve the IM3. It can be further quantified by fitting the measured gain variation to a logarithmic function. The gain, g_1 will have an exponential variation with drain voltage, Vd, as in the expression (1) below.

$$g_1 = \alpha \exp(\beta V_d) \tag{1}$$

where α and β are the constants extracted from the decibel scale measurements.

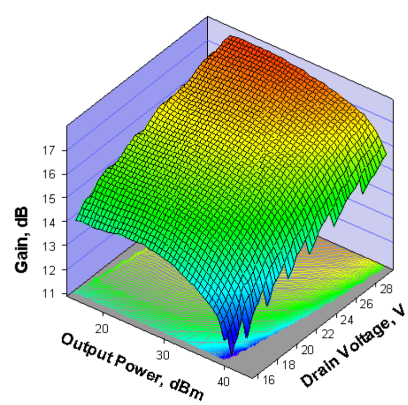

Fig. 1. Gain performance over varying drain voltages

Assume this GaN HEMT power amplifier device has non-linear transfer characteristic of (2) and the drain voltage, Vd is tracking the envelope of input signal, v_{in} (3).

$$i_o = g_1 v_{in} + g_2 v_{in}^2 + g_3 v_{in}^3 + \ldots \tag{2}$$

$$V_d = \delta v_{in} \,. \tag{3}$$

Substituting equation (3) to (1) and inserting back to (2), expanding the equation using an exponential series and limiting the interest up till the third degree, then, the output current, i_o will be simplified into the following equation (4).

$$i_o = \alpha\left(1 + \beta\delta v_{in} + \frac{(\beta\delta v_{in})^2}{2!} + \frac{(\beta\delta v_{in})^3}{3!}\right)v_{in} + g_2 v_{in}^2 + g_3 v_{in}^3 \tag{4}$$

$$i_{o3} = \left(\frac{\alpha\beta\delta}{2} + g_3\right)v_{in}^3 \,. \tag{5}$$

Since the source of IM3 distortion is caused primarily by the third-degree component, equation (5), the tracking voltage characteristic open up a possibility, through the appropriate selection of values of α, β, and δ for cancellation of the IM3, given that g_3 is usually negative.

More simply stated, the inherent device compression characteristic can be cancelled by the expansive gain that is provided by the increasing drain voltage. This offers a linearizing approach that requires an increasing supply voltage at higher drive levels and a decreasing supply voltage at lower drive levels, much like regular ET. The difference here is that AET has the potential to linearize with little or no overall efficiency degradation.

Fig. 2. The implemented Integrated AET Block

III. Integrated AET Block

The AET integrated block consists of an RFPA, a diplexer and an envelope amplifier. The implemented integrated AET block is shown in Fig. 2.

In this AET system, the amplified tracking envelope voltage is superimposed on to fixed DC bias to produce the AET signal that will be the drain supply of the RFPA. The AET signal has a varying drain voltage and results in improved linearity of the power amplifier.

A. RFPA: 25W GaN HEMT Class AB Power Amplifier

The RFPA used in the Integrated AET block employs a 25W GaN HEMT transistor. The RFPA is then designed using microstrip elements to give input and output impedance matching. This transistor is biased in Class AB mode and has fundamental matching with the second harmonic shorted. The maximum measured forward gain, S21 is about 19dB at drain bias of 30V and this RFPA achieved more than 10dB gain across more than 1 GHz bandwidth as shown as in Fig. 3.

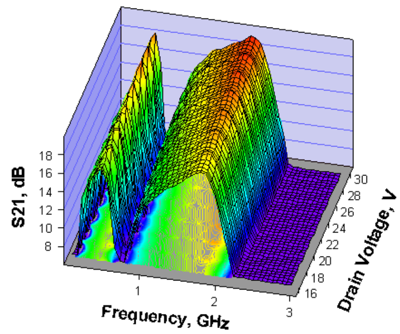

Fig. 3. The forward gain, S21 across the frequency for 25W GaN HEMT Class AB PA.

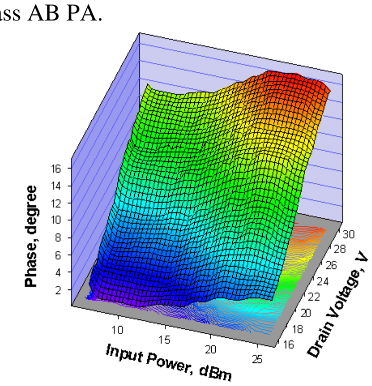

Fig. 4. AM-PM measurement for 25W GaN HEMT Class AB PA

The AM-PM measurement shows that the RFPA is well behaved as the phase changes across input power at maximum of about 6 degree at fixed drain voltage of 30V as shown in Fig. 4. The drain efficiency measured remains high at different value of drain voltages as shown in Fig. 5.

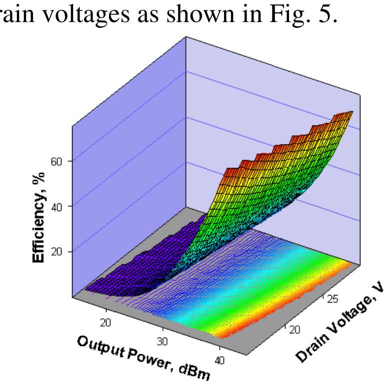

Fig. 5. The drain efficiency of the RFPA over varying drain voltages

978-1-61284-757-3/11/$26.00 C2011 IEEE

B. Diplexer and Envelope Amplifier

The second element in the integrated AET block is the diplexer, and the schematic is shown in Fig. 6(a). The implemented diplexer consists of passive capacitors and inductors and has three ports.

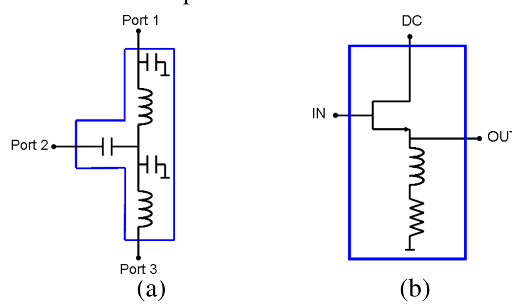

Fig. 6. (a) The diplexer and (b) the envelope amplifier schematics

The diplexer is designed to allow a signal of frequency 100 kHz and above to pass from Port 2 to Port 3, and to pass DC from Port 1 to Port 3.

The envelope amplifier is the final part of the integrated AET block, and is shown schematically in Fig.6 (b). This envelope amplifier is designed using a source follower amplifier configuration to achieve a low output impedance at baseband frequency. The low output impedance is required to achieve voltage source functionality. A large inductor is directly connected to the source of the n-channel FET and a small value resistor is connected between the inductor and the ground. The combination of these two passive components maintains the minimum required DC current flowing through the transistor. The lowest possible DC current is required to maintain high efficiency for the RFPA in AET system.

IV. AET EXPERIMENTAL SETUP

The AET experimental setup for 2-carrier signal measurement at 1.98GHz with 1MHz spacing is shown in Fig. 7. The 2-carrier signal is generated by two signal generators that are phase-locked and these two continuous wave (CW) signals are combined using a combiner to produce the modulated signal. The amplitude and phase of the envelope signal is emulated using the third signal generator that is also phase-locked with the other generators. The RF signal is amplified by a driver amplifier and then the signal is fed to the RF input of the RFPA. The emulated envelope signal is a sinusoidal signal and this signal is inserted to a bias tee. A dc component is combined with the emulated envelope signal through a bias tee. A DC component is needed to turn on the n-channel FET and bias this transistor into saturation to perform as a voltage source. This emulated envelope signal is inserted to an envelope amplifier and this signal is combined with a DC component through a diplexer. The resulted AET signal will bias the RFPA.

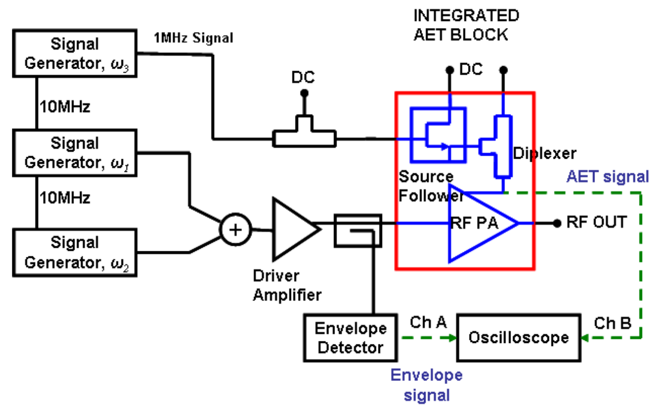

Fig. 7. The AET experimental setup

V. MEASUREMENT RESULT

During the measurement the AET signal and the envelope signal waveforms were observed on an oscilloscope, as shown in Fig. 7 and the waveforms are shown in Fig. 8 (note that the 2-carrier envelope is distorted by the square law detector).

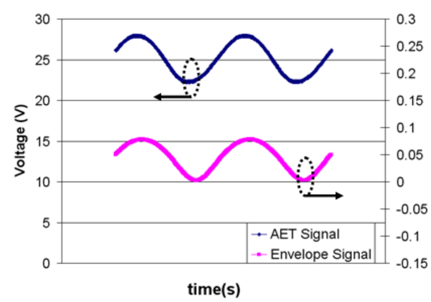

Fig. 8. AET tracking and envelope signal waveforms

The AET signal phase is adjusted so that the AET signal is aligned with the envelope signal so IM3 and IM5 will be symmetrical [2], [3]. The AET amplitude is also adjusted to give optimum IM3 and IM5 performance.

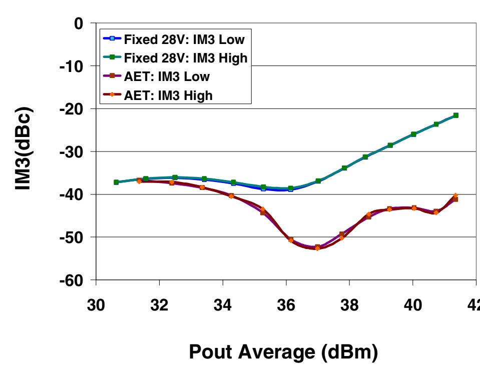

Fig. 9. IM3 performance for AET system and fixed drain bias

The optimum IM3 performance of the RFPA using AET shows a large improvement at higher power level i.e. 18 dB at an average output power of 41dBm. This measurement is

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compared to the RFPA biased at fixed voltage of 28V as shown in Fig. 9. The comparison is done for the RFPA biased at 28V, which is the same as the peak level of the composite AET signal. But it should be noted that the heat dissipation will be much lower in the AET case, raising the possibility of using much higher peak AET voltages than would be allowable with a fixed supply.

The IM5 performance was also measured and the result is shown in Fig. 10. The IM5 of the RFPA operating in the AET system shows that the performance remains low as compared to the RFPA operating on fixed bias.

This AET system confirms the results from measurements that have been performed separately [4] at the device level by emulating baseband impedance at the drain termination.

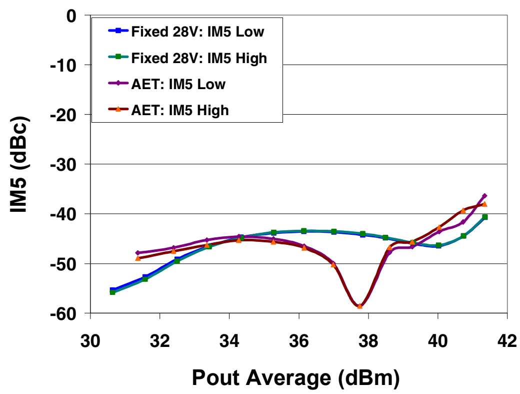

Fig. 10. IM5 performance for AET system and fixed drain bias

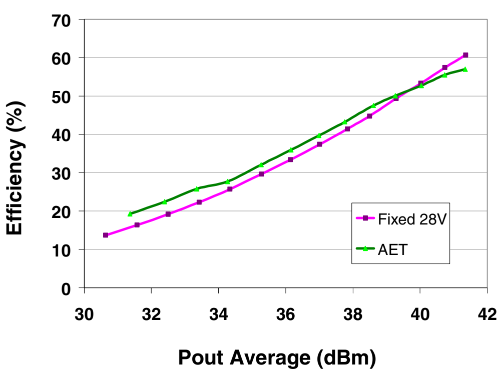

Fig. 11. Drain Efficiency performance for AET system and fixed drain bias

Although the focus of this paper is on the improved linearity, the drain efficiency was also measured and the result in Fig. 11 shows a small improvement in drain efficiency over most of the measured power range. This shows that the linearity improvement observed using AET is obtained with minimal overall reduction in efficiency, even when the power consumption of the linearizer is fully taken into account. We note in passing that published results on other linearization methods, e.g. digital pre-distortion, customarily do not account for the extra power consumption of the linearization.

VI. CONCLUSION

A novel linearization technique called AET has been described. A compact integrated system based on a 25W GaN RFPA device has been demonstrated. IM3 improvement between 10dB and 18dB has been observed over a 10dB power range, with an 18dB improvement at the highest power level. This linearity improvement has been obtained with negligible impact on the overall efficiency of the system. Future work will investigate more complex modulation systems, and possibilities for more substantial efficiency improvement in comparison to single supply operation.

ACKNOWLEDGEMENT

This work has been carried out as part of EPSRC grant EP/F033702/1. The authors would also like to thank CREE for supporting this activity and supplying the devices and Yayasan Telekom Malaysia, Kuala Lumpur for PhD student sponsorship.

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